AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 16, line 23, of the specification with the following rewritten paragraph:

System 10 comprises one or more substantially similar interfaces 26 which receive input/output (IO) access requests for data in disks 12 from hosts 52. Each interface 26 may be implemented in hardware and/or software, and may be located in storage system 10 or alternatively in any other suitable location, such as an element of network 50 or one of host processors 52. Between disks 12 and the interfaces are a second plurality of interim caches 20, each cache comprising memory having fast access time, and each cache being at an equal level hierarchically. Each cache 20 typically comprises random access memory (RAM), such as dynamic RAM and/or solid state disks, and may also additionally comprise software configured to run on a processor in the cache. Caches 20 are coupled to interfaces 26 by any suitable fast coupling system known in the art, such as a bus or a switch, so that each interface is able to communicate with, and transfer data to and from, any cache. Herein the coupling between caches 20 and interfaces 26 is assumed, by way of example, to be by a first cross-point switch 14. Interfaces 26 operate substantially independently of each other. Caches 20 and interfaces 26 operate as a data transfer system 27, transferring data between hosts 52 and disks 12.